**Basic Electrical Science Lab  
Course Code: EE152**

**Laboratory Manual**

Name: Sadat Zubin Aftab Shah

Roll No: 20CSE1030

Section: B

Academic Session: April – August 2021

**National Institute of Technology Goa**



**CERTIFICATE**

This is to certify that Mr./ Ms. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ of Class B.Tech 1st year (2nd Sem), Division Sec A/B, bearing Roll. No.\_\_\_\_\_\_\_\_\_\_\_\_\_, has satisfactorily completed the course experiments in the Laboratory Course Basic Electrical Science Lab (EE152) in the academic year 2020-2021 in the Institution of National Institute of Technology Goa.

**Course Instructor**

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**Experiment 1**

**Verification of Ohms Law**

1. **Aim**: To verify Ohms Law for the given circuit
2. **Software tools required:** MATLAB/SIMULINK
3. **Simulink Block sets Used:** Powergui, DC Voltage Source, Series RLC Branch, Current Measurement, Voltage Measurement, Display, Scope, XY Graph, Controlled Voltage Source, Ramp, Group 1 signal builder
4. **Theory**: Ohms Law states that the voltage across conducting materials is directly proportional to the current through the material. one arrives at the usual mathematical equation that describes this relationship

V α I

* V = IR

Where, V – Voltage across the element

I – Current flowing through the element

R - Resistance offered by the element

R is also the slope of the straight line when V-I characteristics are plotted. Normally resistance is a positive quantity.

1. **Circuit Diagram:** The considered circuit for Ohms law verification is as given in fig. 1a. The connected circuit in MATLAB/Simulink is given in Fig.1b.

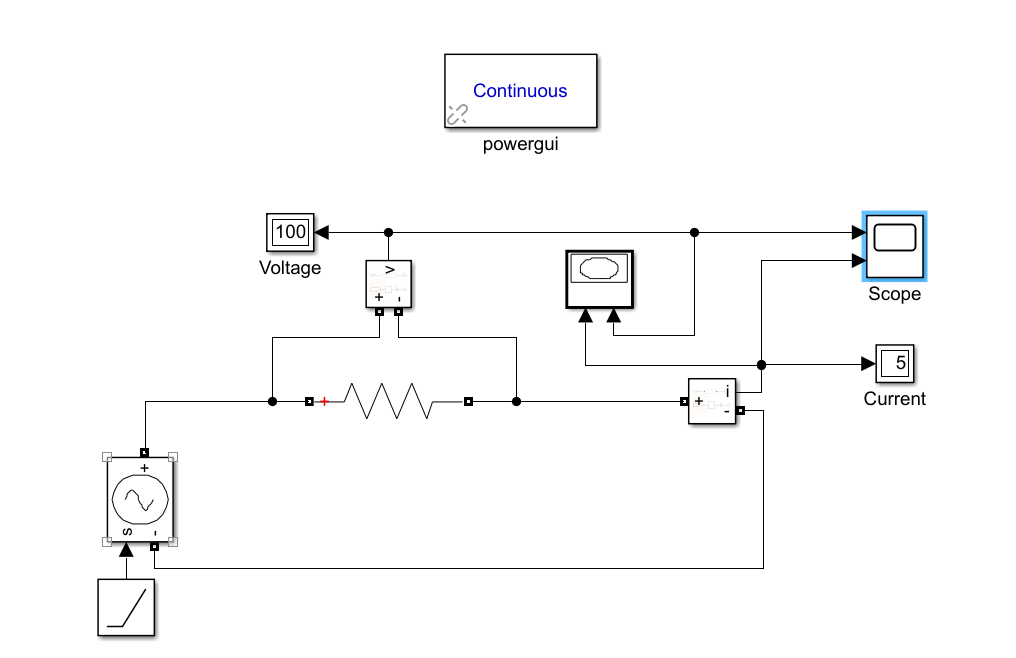
100 V

20 Ω

(0-5 A)

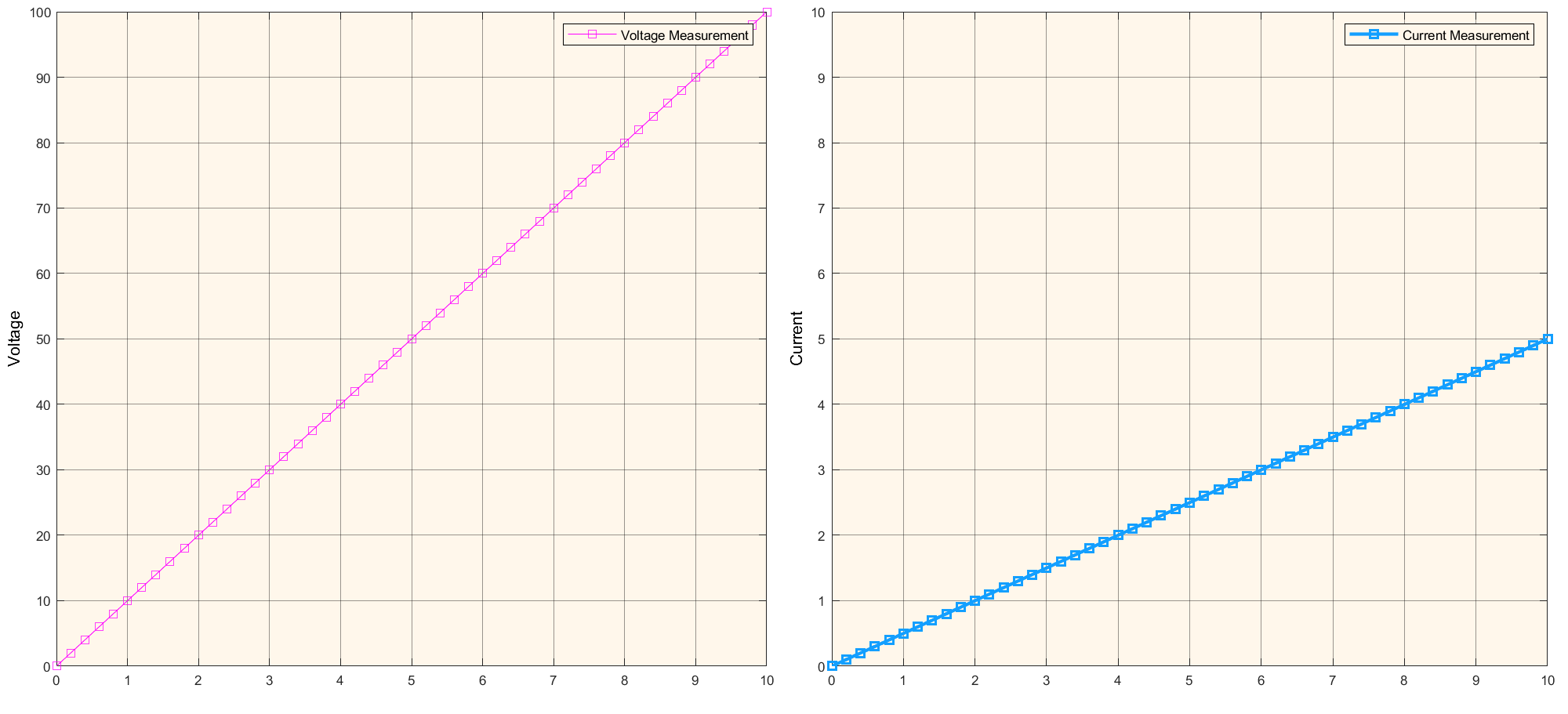
(0-100 V)

**Fig1a**: Circuit Diagram

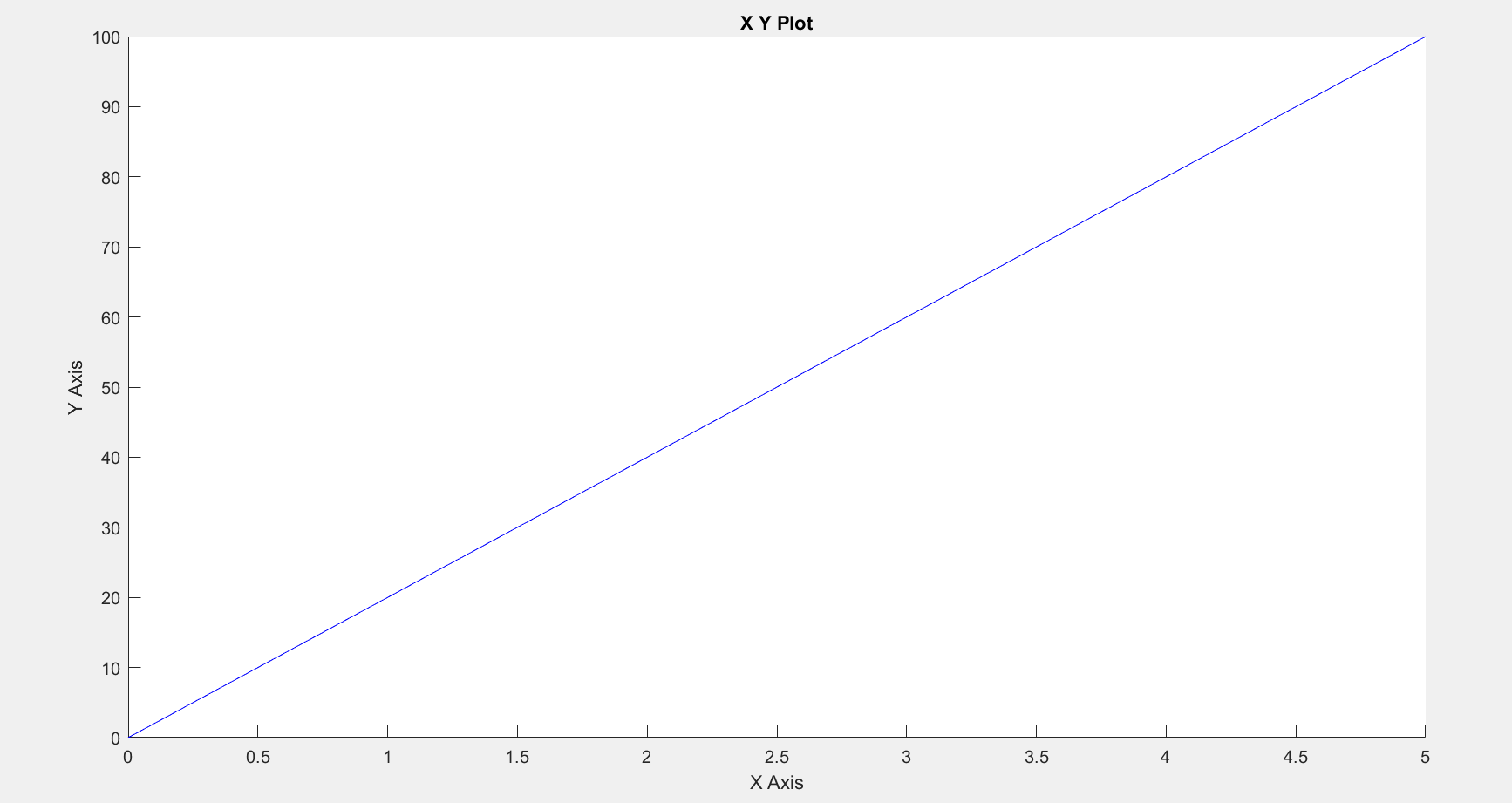


**Fig1b**: Circuit connections in Simulink

1. **Procedure:**
2. The mentioned Simulink blocksets are connected as shown in Figure 1b.
3. Apply the specified voltage across the specified resistance
4. Measure the current flowing through the resistor
5. V-t, I-t and V-I plots are generated
6. The same procedure is repeated for specified types of inputs like Constant DC, Ramp, etc.
7. **Graphical Results:**

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**Fig.1c:** Voltage Vs Time and Current Vs time Plots

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**Fig1d:** V-I Characteristics

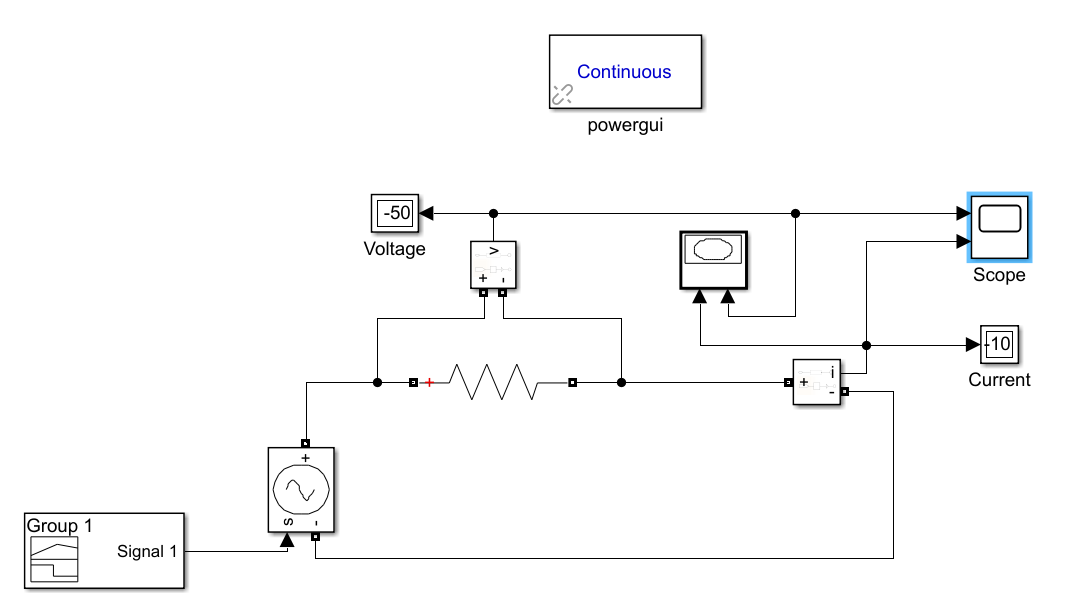
1. **Precautions:**
2. Ensure that ‘Powergui’ block set is included in the Simulink file.
3. Ensure that connections are properly made.
4. Ensure that the scale of the graphs should be adjusted to the range in which the readings vary.
5. **Inferences**: From the output, it can be inferred that as the input ramp is varied from 0-100 V, the current through the resistance varies from 0-5 A.
6. **Conclusion:** The Ohms law is verified for all the specified inputs for the studied resistive network.

**Assignment:**

* 1. Consider the below Step function as input with R = 5Ω

V(t) = 50V 0 ≤ t ≤ 5 sec

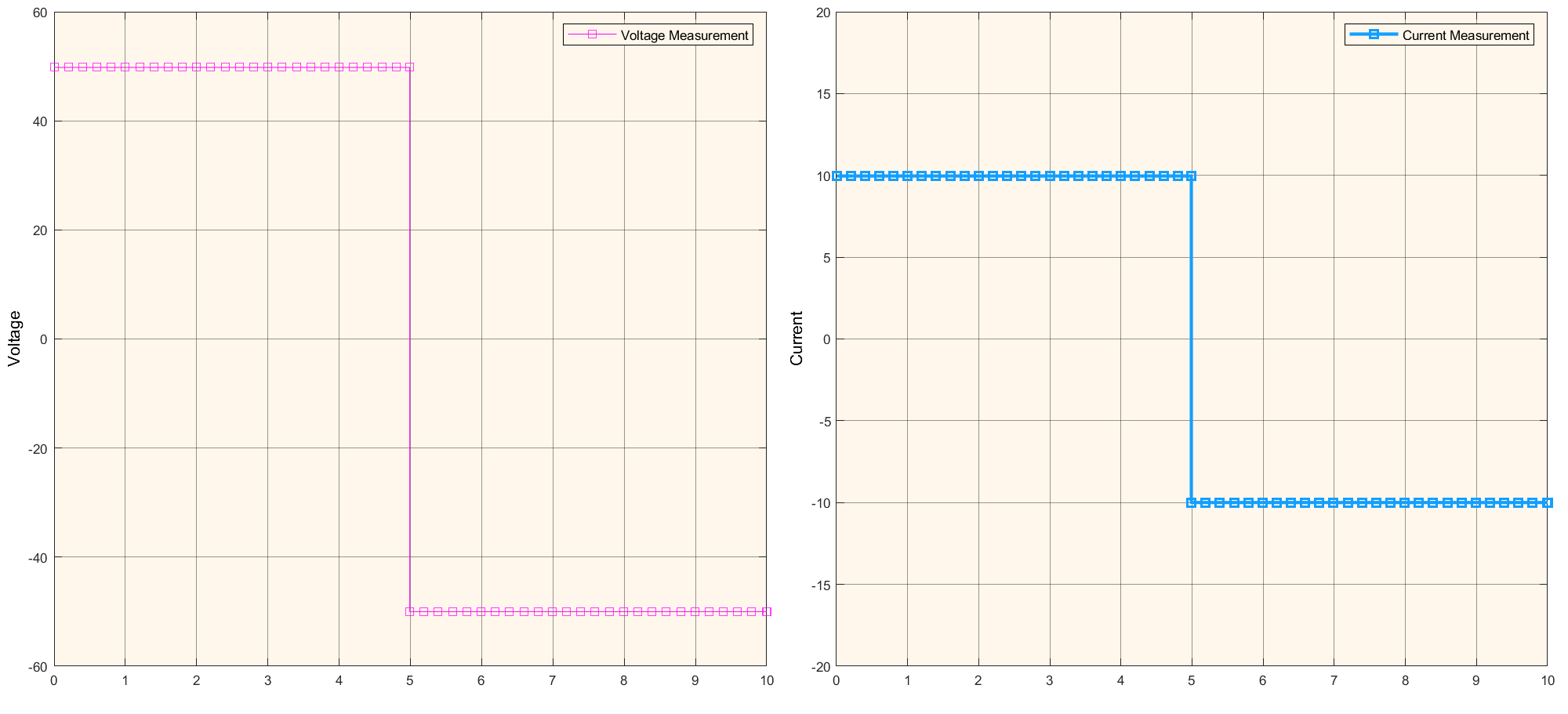
= -50V 5 ≤ t ≤ 10 sec



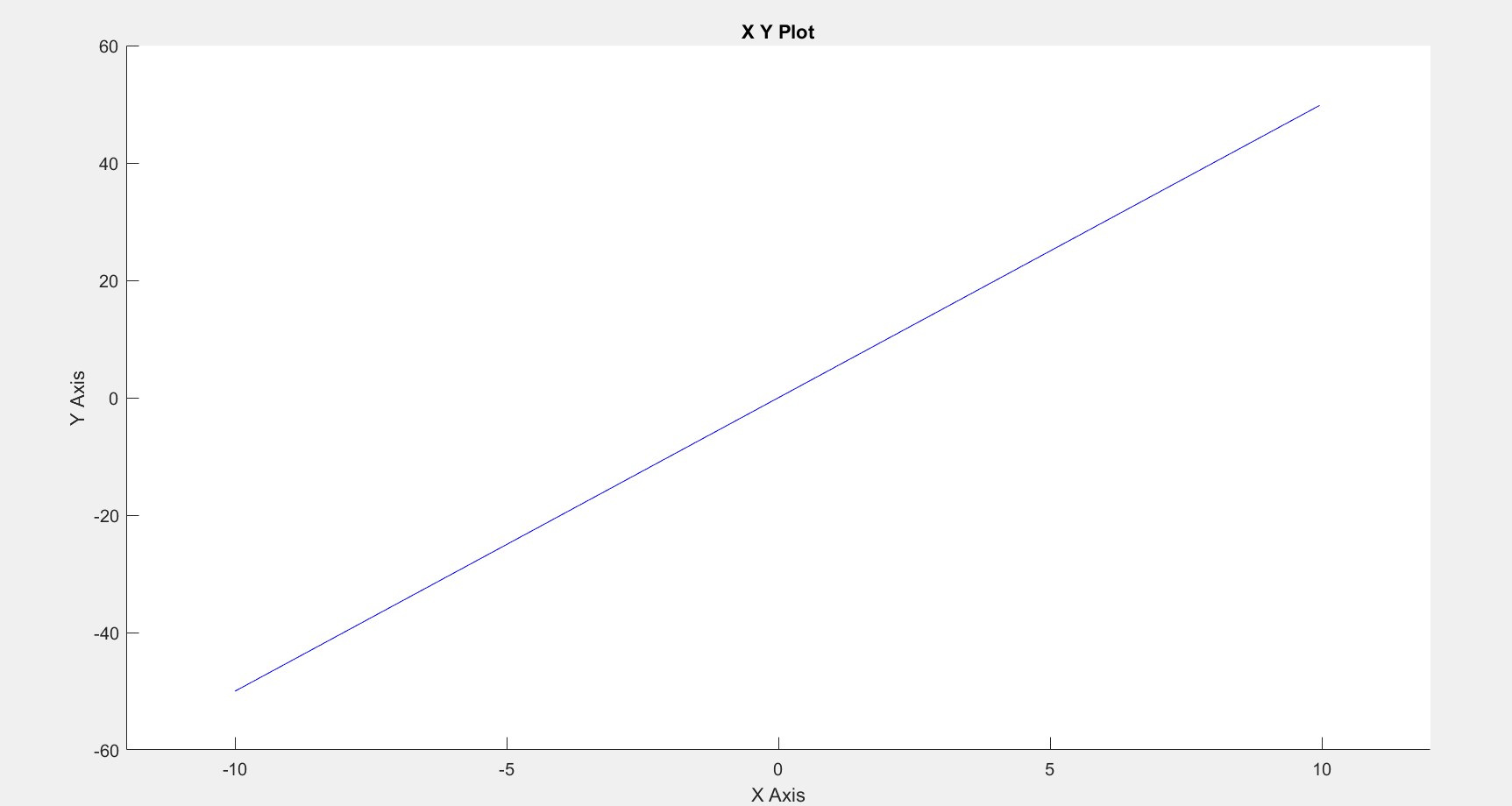
**Fig1e**: Circuit connections in Simulink

**Procedure:**

1. The mentioned Simulink blocksets are connected as shown in Figure 1e.
2. Connect the Group 1 signal builder with the controlled voltage source to apply the specified voltage across the specified resistance.
3. Measure the current flowing through the resistor.
4. V-t, I-t and V-I plots are generated.



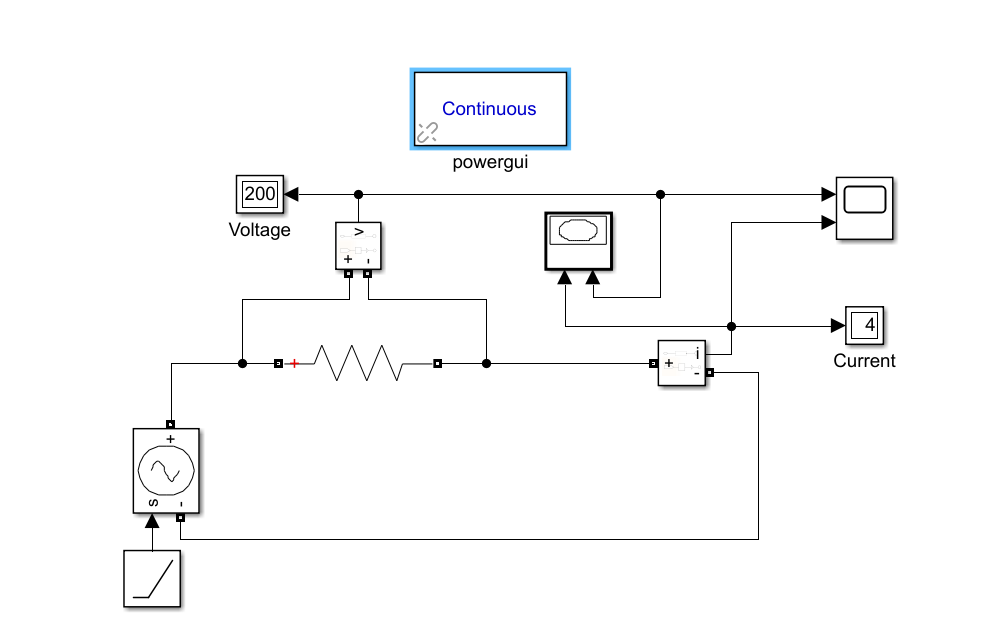
**Fig.1f:** Voltage Vs Time and Current Vs time Plots



**Fig1g:** V-I Characteristics

**Inferences:** From the output, it can be inferred that, as the input voltage is fixed at 50V in first half of simulation, the current remained fixed at 10A and in the second half as the input voltage is fixed at  
-50V the current remained fixed at -10A, keeping the V/I ratio constant throughout the simulation.

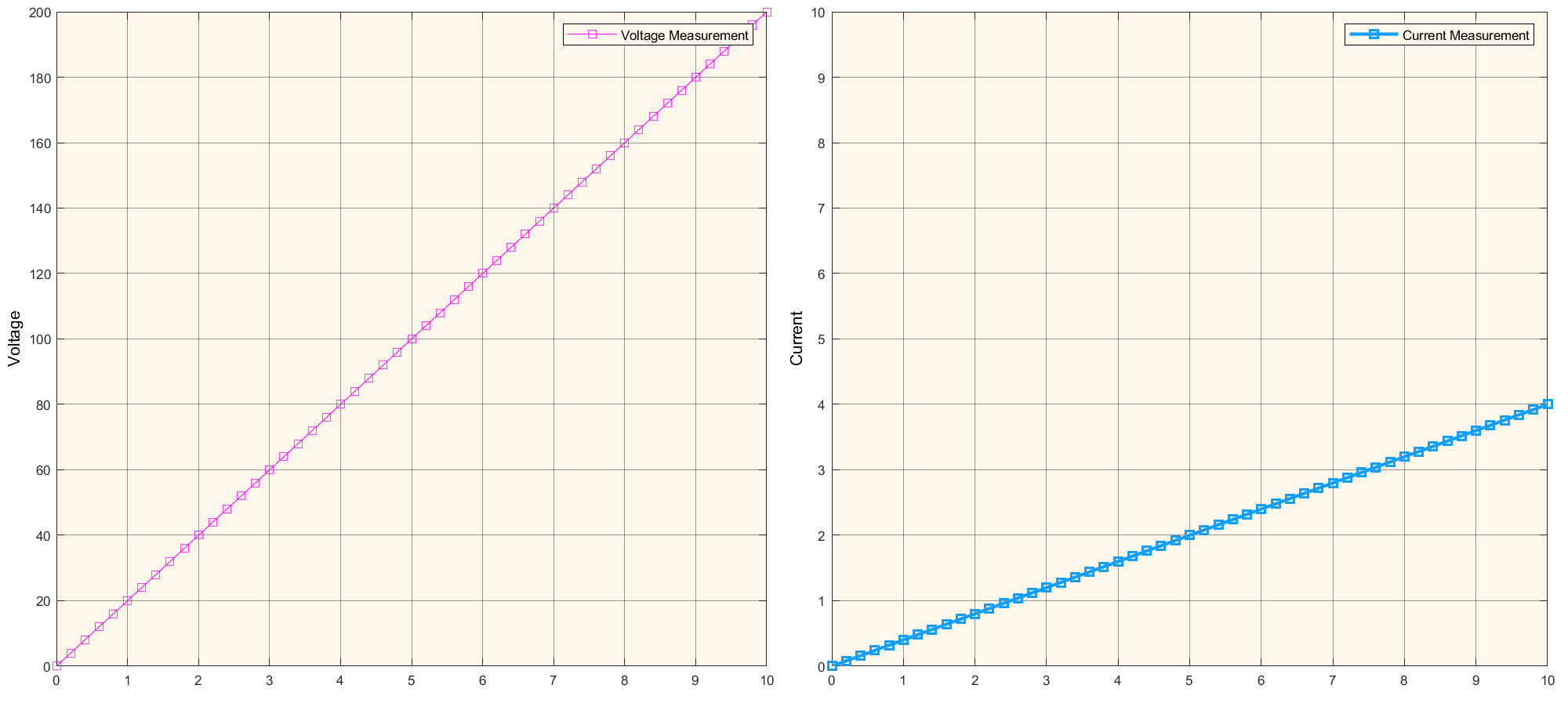
* 1. Consider the Ramp function varying from 0-200 V as input with R = 50Ω



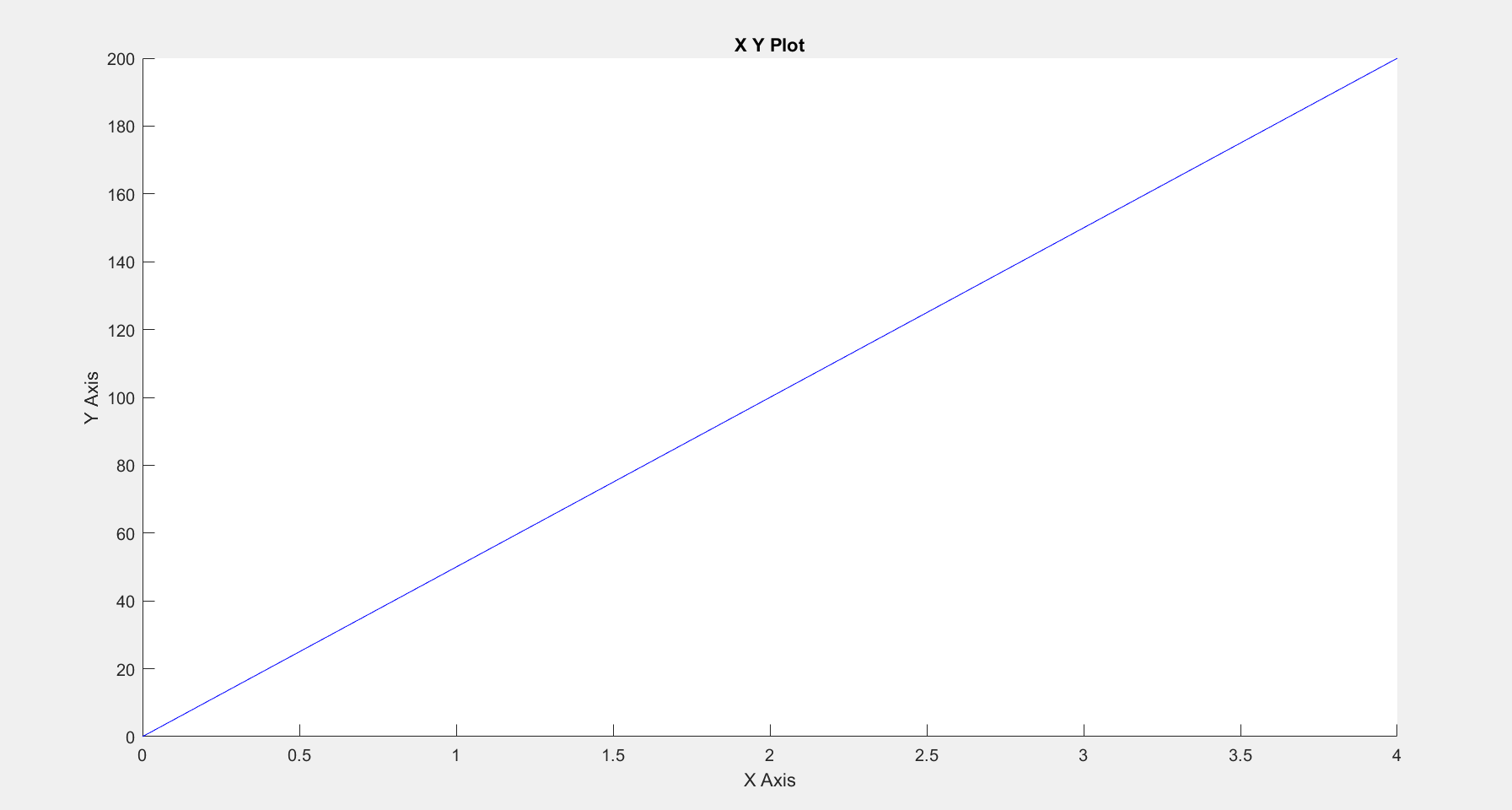
**Fig1h**: Circuit connections in Simulink

**Procedure:**

1. The mentioned Simulink blocksets are connected as shown in Figure 1h.
2. Connect the ramp blockset with the controlled voltage source to apply the specified voltage across the specified resistance.
3. Measure the current flowing through the resistor.
4. V-t, I-t and V-I plots are generated.



**Fig:1i**: Voltage Vs Time and Current Vs time Plots



**Fig1j:** V-I Characteristics

**Inferences**: From the output, it can be inferred that as the input ramp is varied from 0-200 V, the current through the resistance varies from 0-4 A.

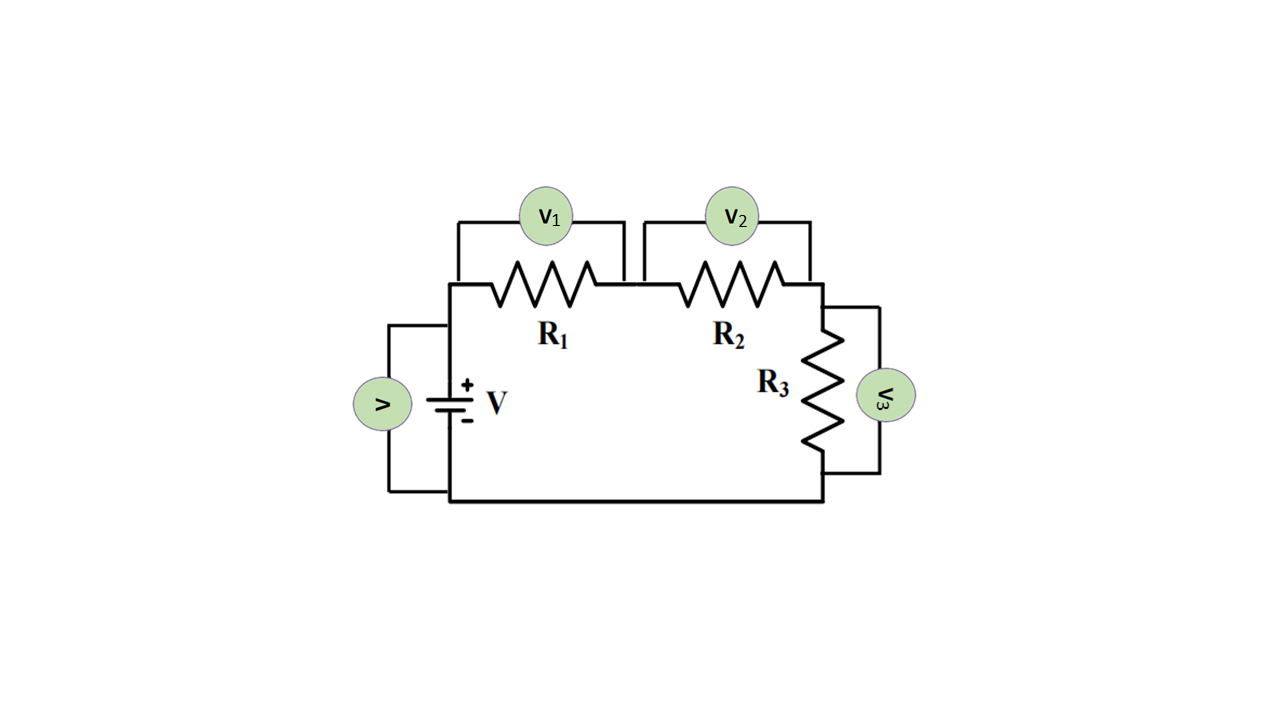
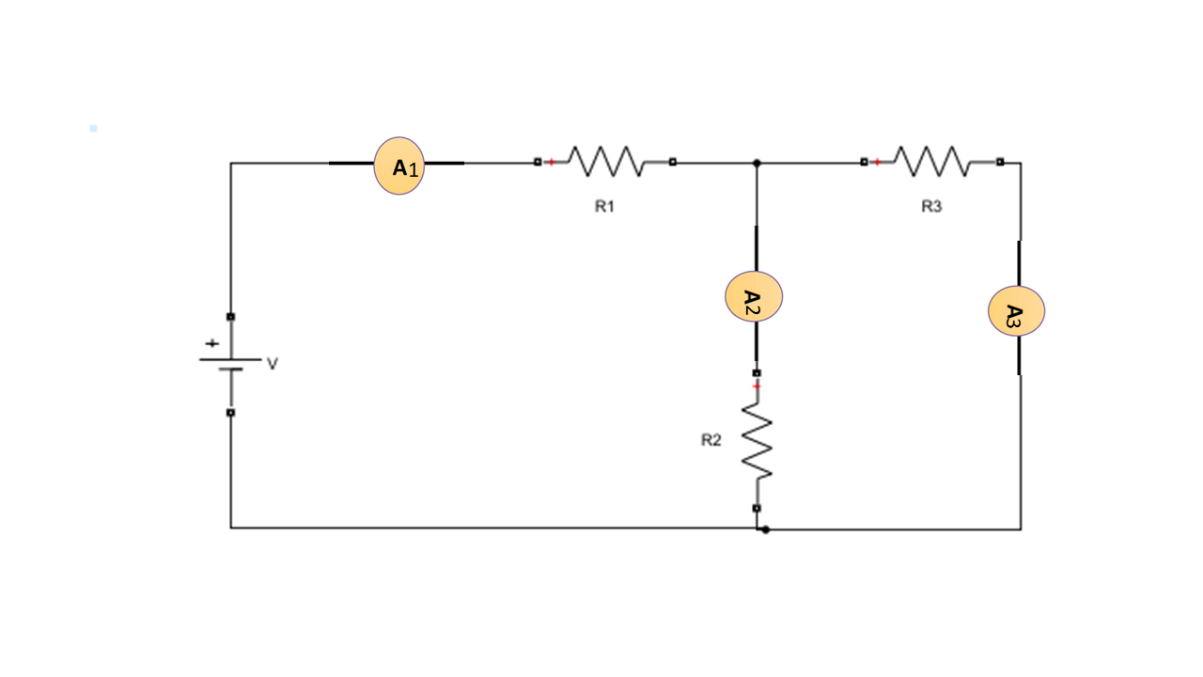
­­ **Experiment 2**

**Verification of Kirchhoff's Laws – KVL and KCL**

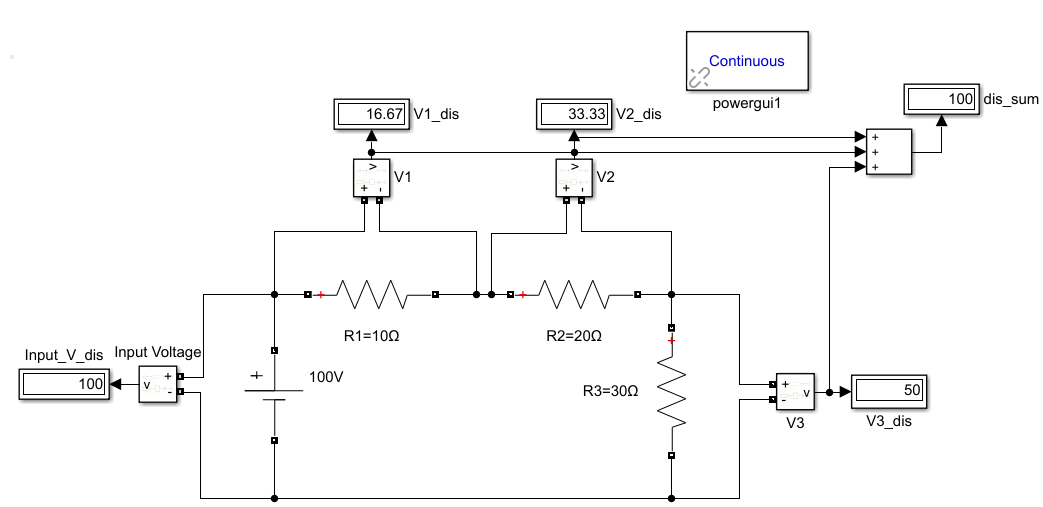
1. **Aim**: To verify Kirchoff’s voltage law and Kirchoff’s current law for the given circuit.
2. **Software tools required:** MATLAB/SIMULINK
3. **Simulink Block sets Used:** Powergui, DC Voltage Source, Series RLC Branch, Current Measurement, Voltage Measurement, Display, Scope, XY Graph, Controlled Voltage Source, Ramp, Group 1 signal builder,
4. **Theory:** Kirchoff's voltage law states that the algebraic sum of the potential differences in any loop must be equal to zero. Mathematically, ΣV = 0 where V is the potential difference between a loop element. KVL deals with conservation of energy.

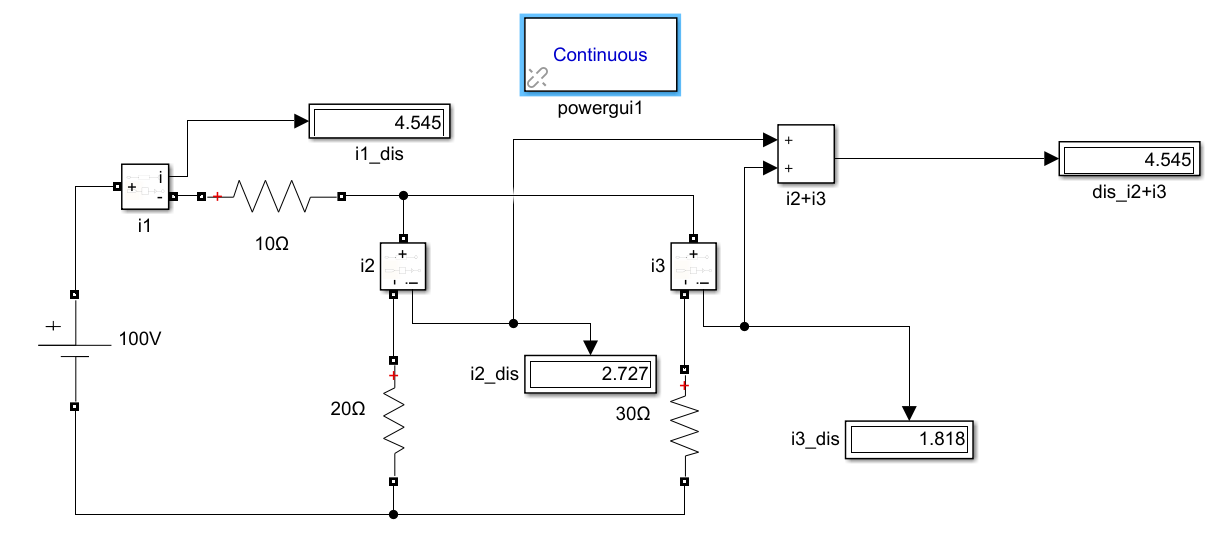
Kirchoff’s current law states that current entering a node is equal to current leaving the node.  
Mathematically, ΣI = 0, where I is the current entering the node from a particular direction.

1. **Circuit Diagram:** The considered circuit for Kirchoff Voltage law verification is as given in fig. 2a. The considered circuit for Kirchoff Current law verification is as given in fig. 2b. The connected circuit of KVL and KCL in MATLAB/Simulink is given in Fig.2c and Fig.2d.

**Fig2a**: Circuit Diagram for KVL **Fig2b**: Circuit Diagram for KCL

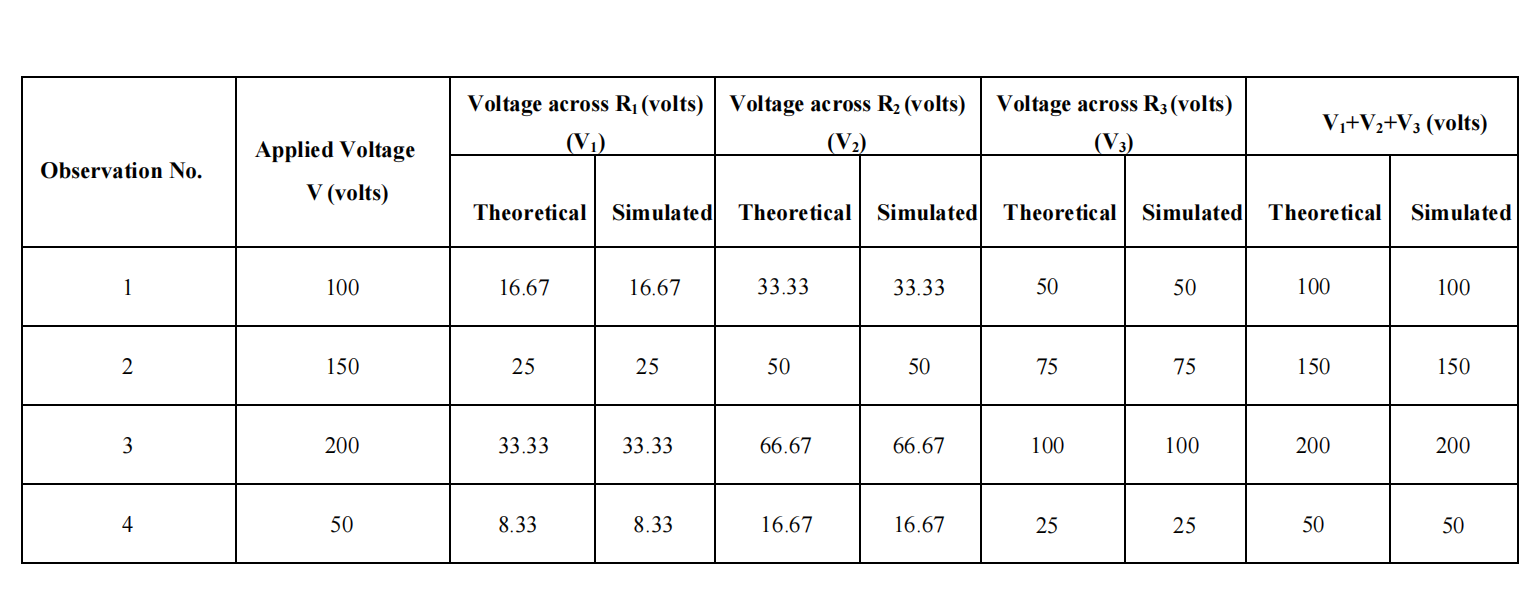
  
**Fig2c**: Circuit connections in Simulink for KVL

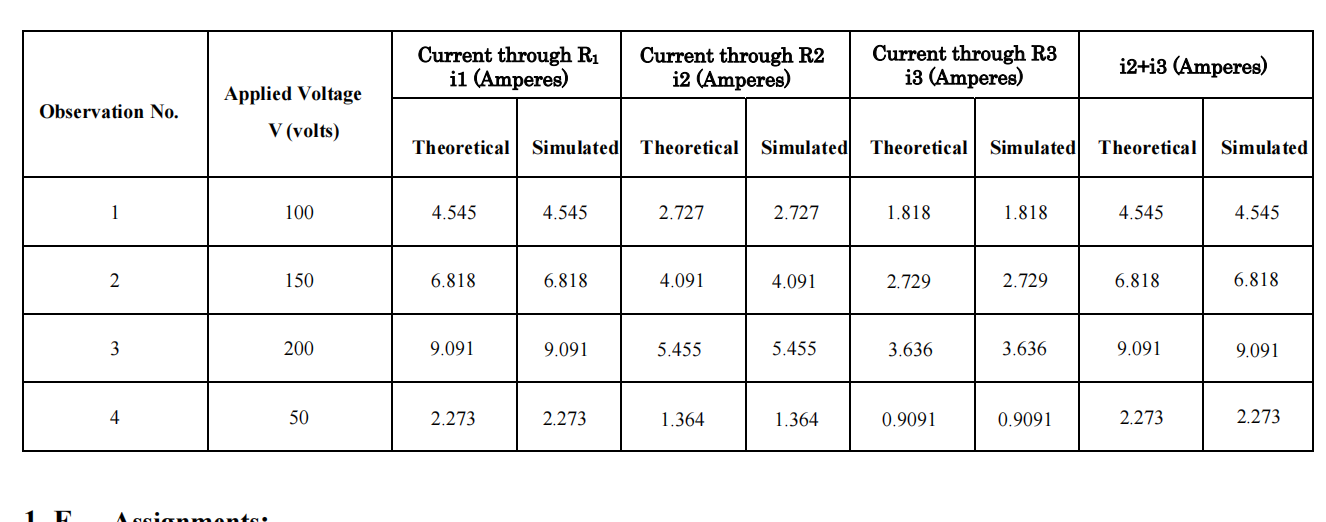
  
**Fig2d**: Circuit connections in Simulink for KCL

1. **Procedure:**
2. Convert the circuit shown in Fig. 2 into experimental circuit (necessary measuring   
   instruments are to be incorporated in the circuit).
3. Construct the experimental circuits in MATLAB/Simulink domain, and simulate it.
4. Based on the simulation, fill up the Table-2.1 for KVL. Similarly, prepare a table for KCL

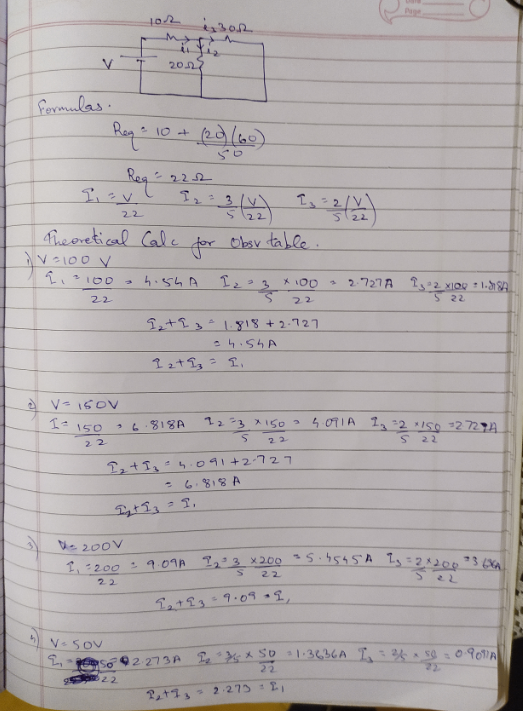
experiment, and fill it.

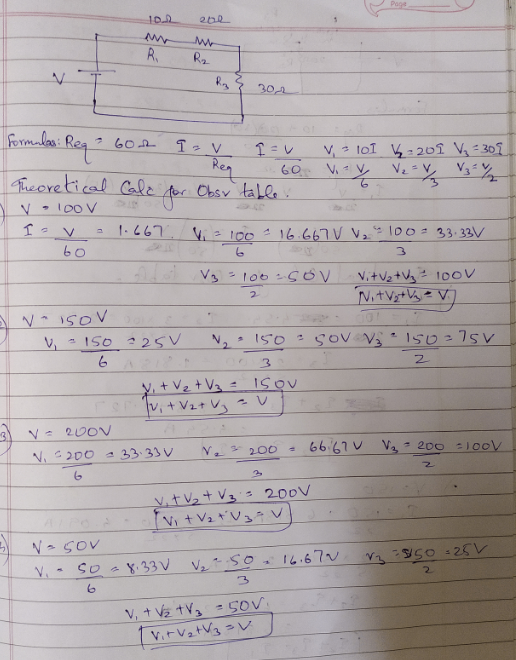
1. **Observations:**

**Table 2.1:** Observation table for KVL



**Table 2.2:** Observation table for KCL

1. **Theoretical Calculation Working**:



1. **Precautions:**
2. Ensure that ‘powergui’ block set is included in the Simulink file.
3. Ensure that connections are properly made.
4. Ensure that the scale of the graphs should be adjusted to the range in which the readings vary.
5. **Inferences:**

* From the observation table 2.1, it can be inferred that sum of V1+V2+V3 is always equal to V.
* From the observation table 2.2, it can be inferred that sum of i2+i3 is always equal to i1.
* All the theoretical readings match with the simulated readings.

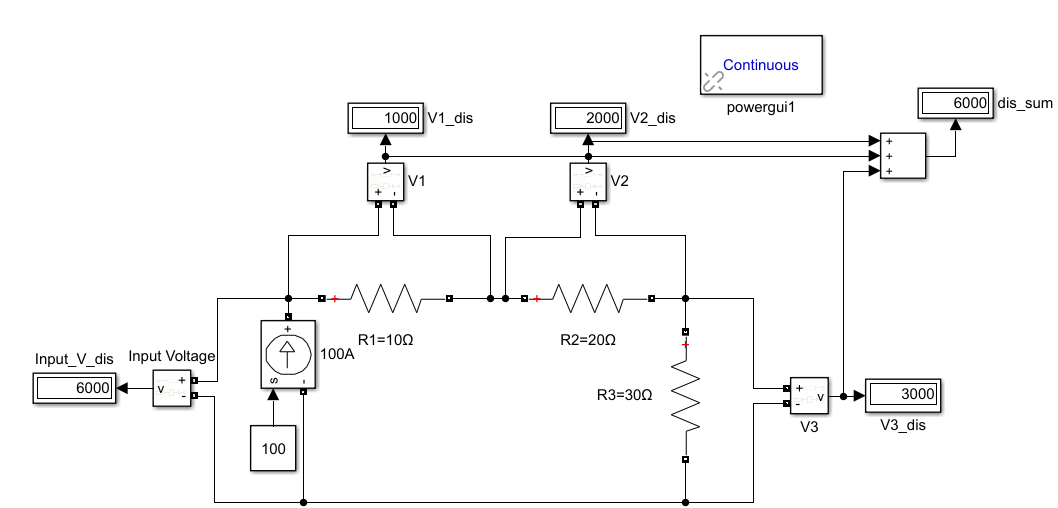
1. **Conclusion:**

* Kirchoff’s voltage law and Kirchoff’s current law are hence verified.

**Assignment:**

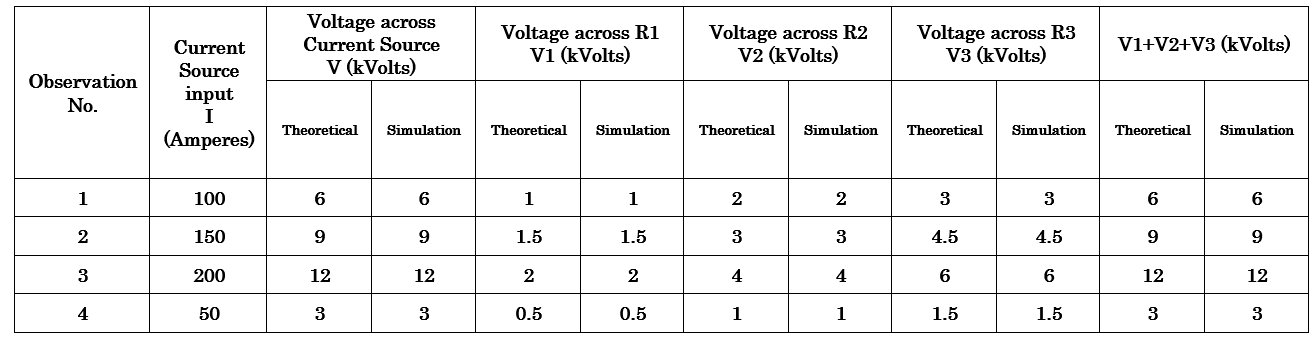
1. Replace constant voltage source by constant current source with the same magnitude in Fig. 2.a & 2.b, do the simulation again.

**Circuit Diagram:**

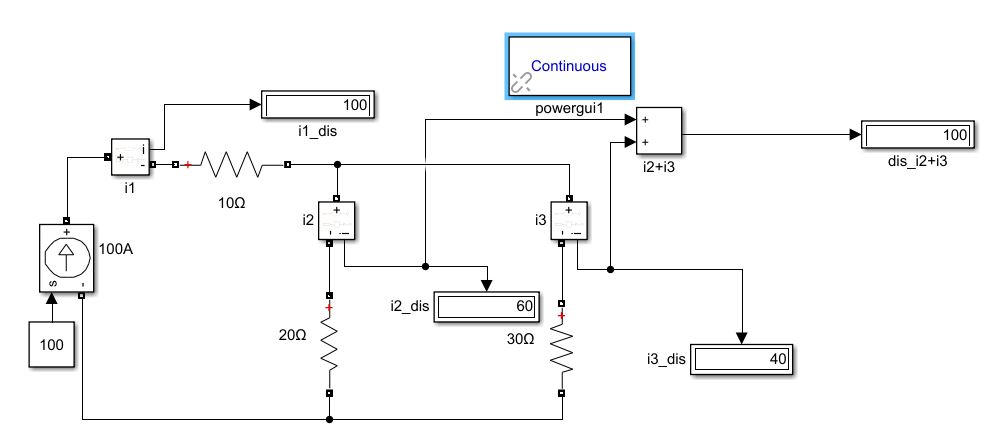
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**Fig2e**: Circuit connections in Simulink for KVL with constant current source

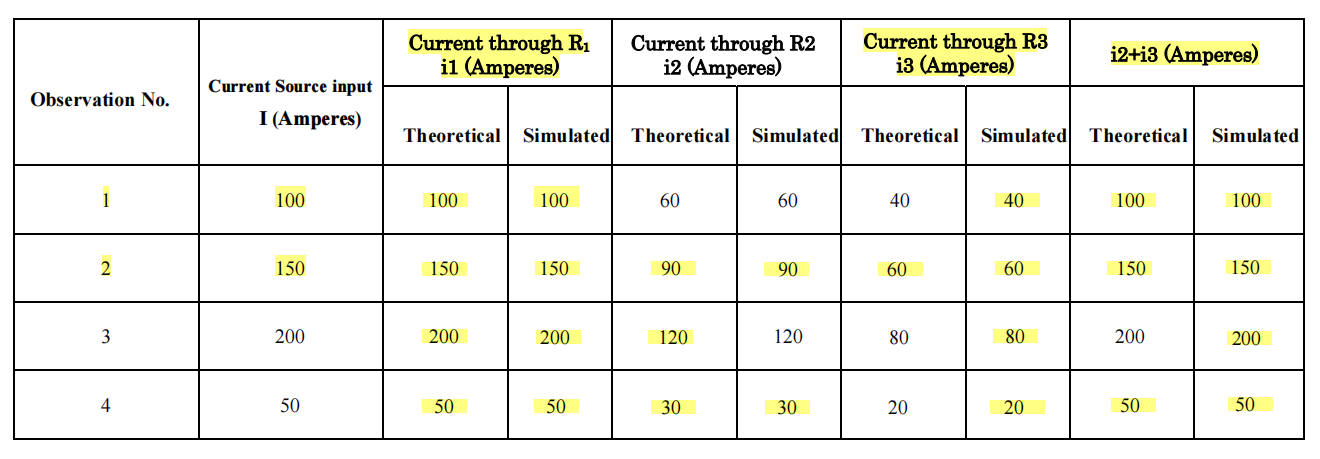
**Observations:**



**Table 2.3:** Observation table for KVL using constant current source

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Fig2f**: Circuit connections in Simulink for KCL with constant current source

**Observations:**

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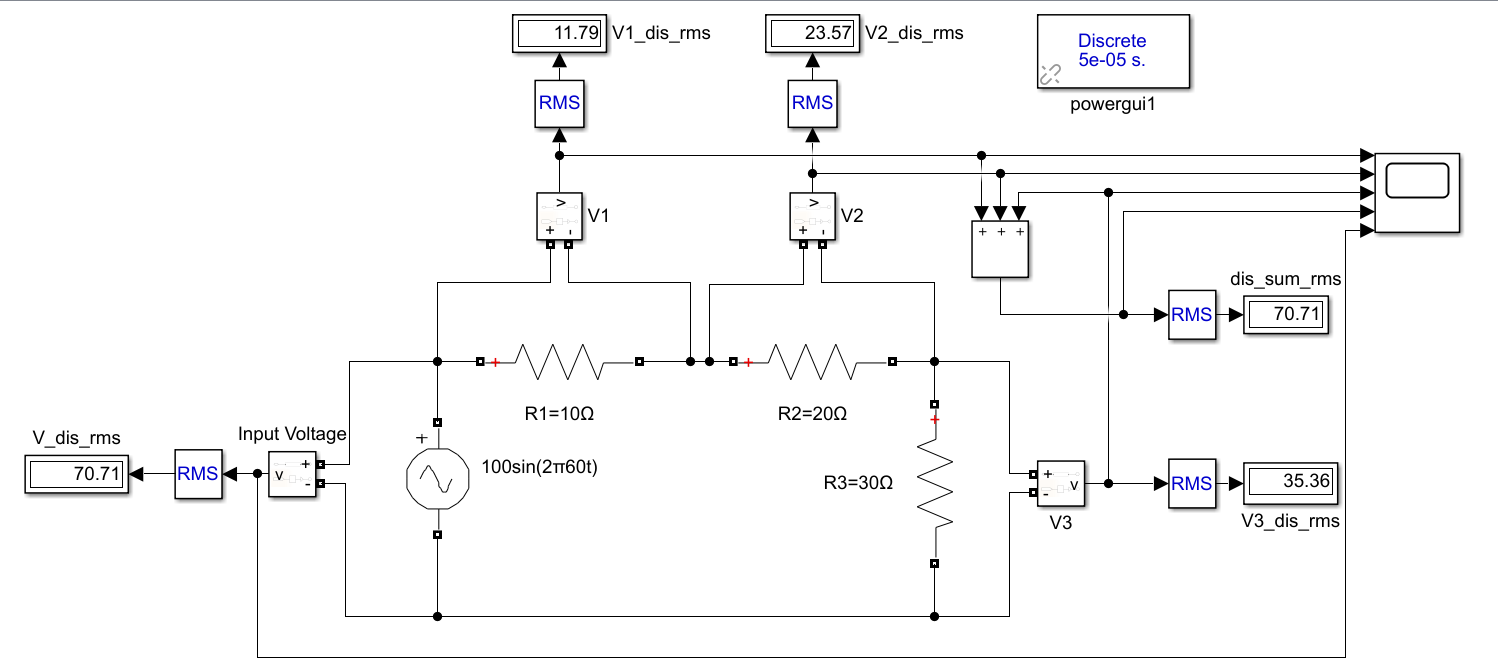
**Table 2.4:** Observation table for KCL using constant current source

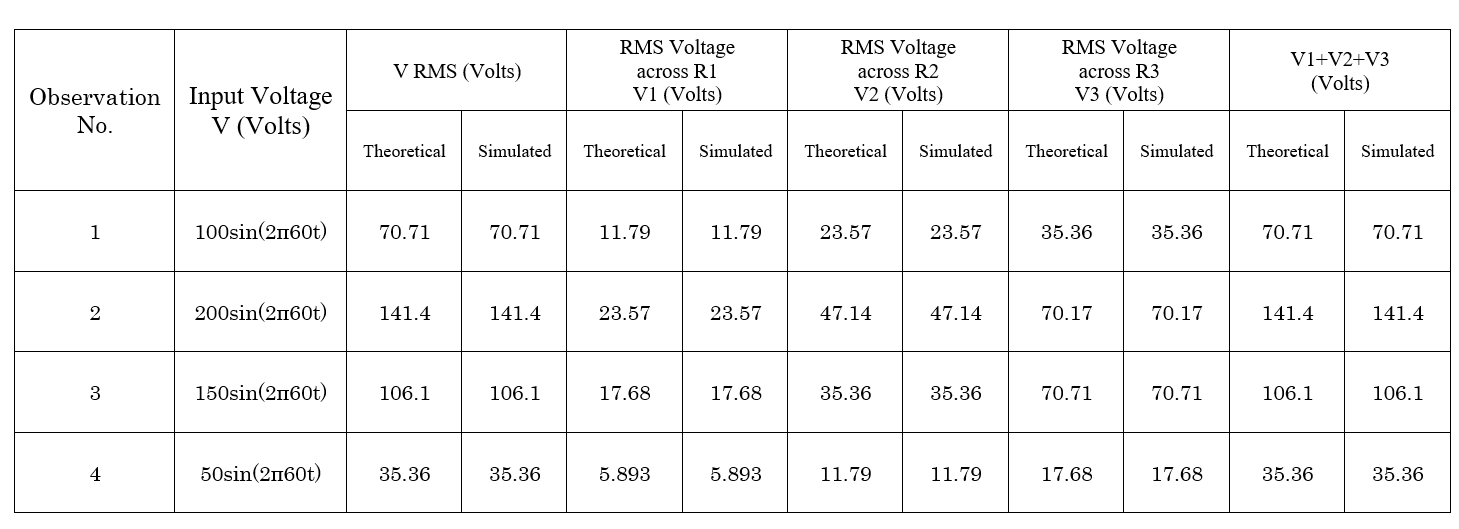
**Inferences:**

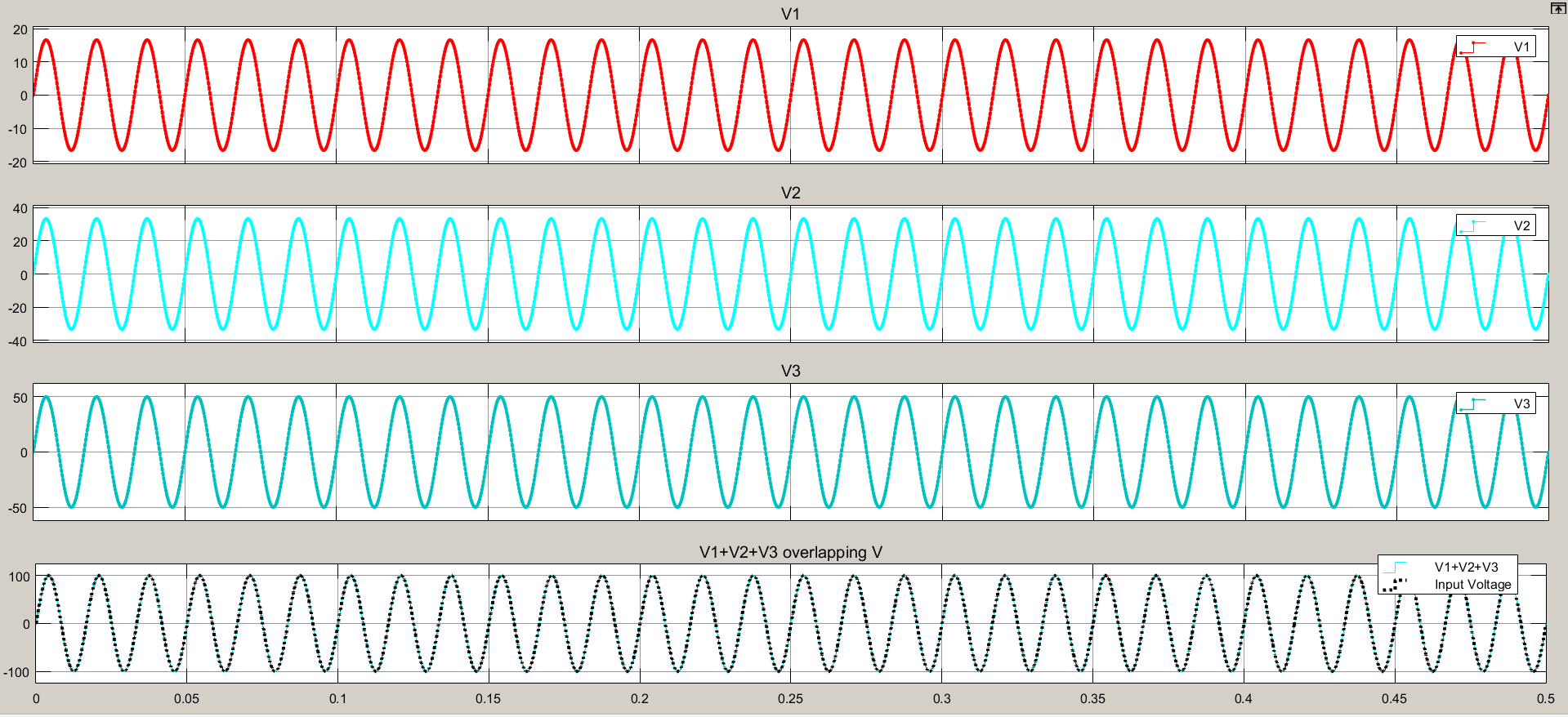
* From the observation table 2.3, it can be inferred that sum of V1+V2+V3 is always equal to V.
* From the observation table 2.4, it can be inferred that sum of i2+i3 is always equal to i1.
* All the theoretical readings match with the simulated readings.
* KCL and KVl is verified using constant current source.

1. Replace constant voltage source by variable voltage source (sinusoidal source with the same

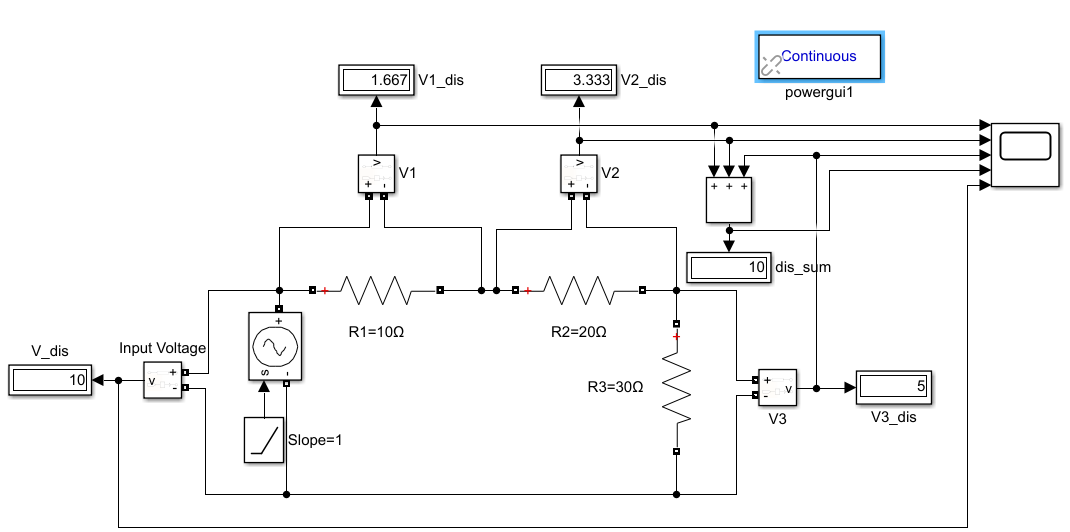
magnitude, ramp input with slope 1) in Fig. 2.a & 2.b, do the simulation again.



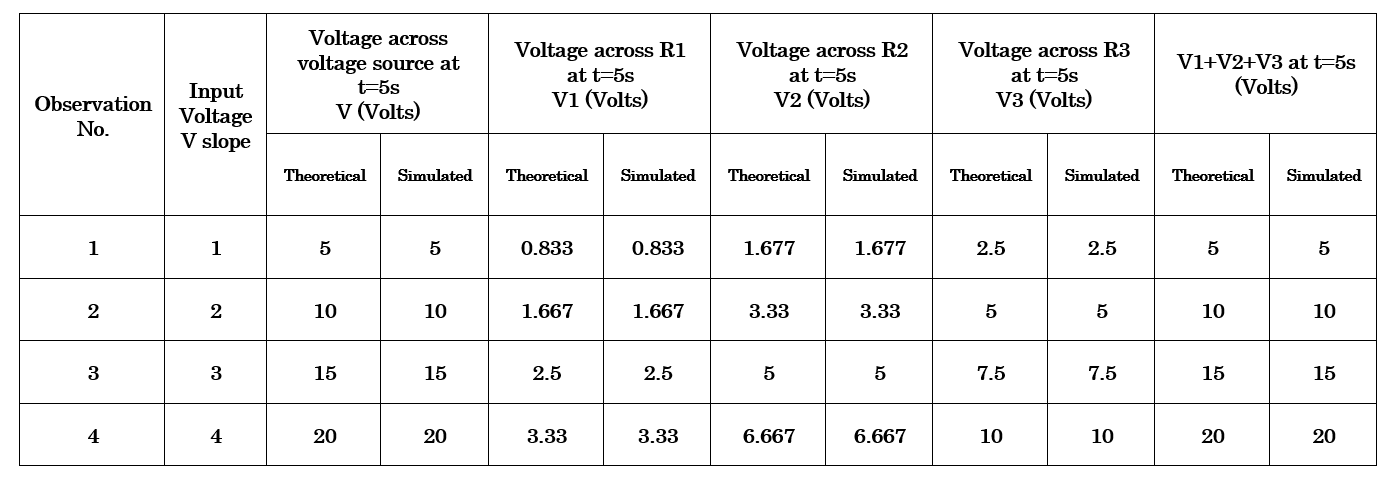
**Fig2g**: Circuit connections in Simulink for KVL using sinusoidal voltage source **Table 2.5:** Observation table for KVL using sinusoidal voltage source

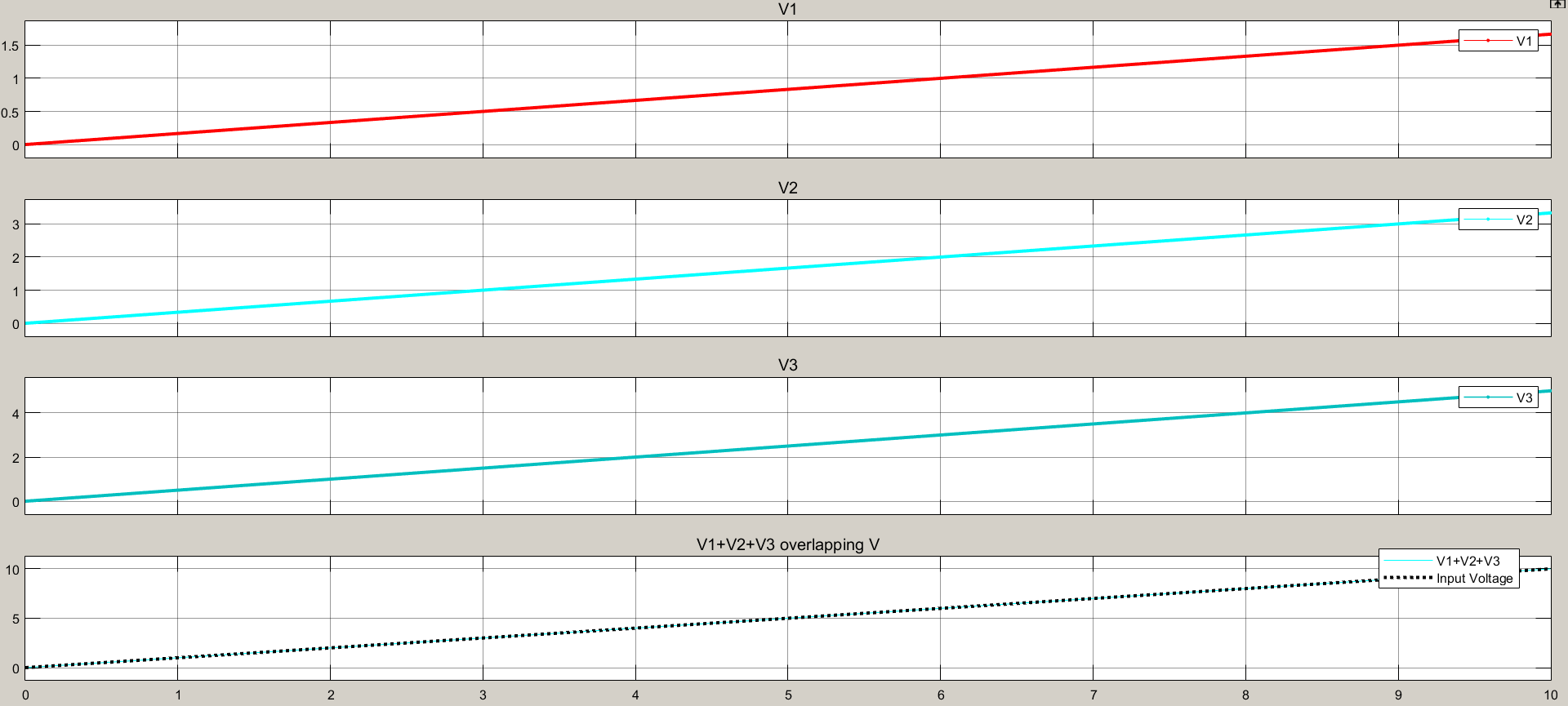


**Graph 2.1:** Graphical results of KVL using sinusoidal voltage source

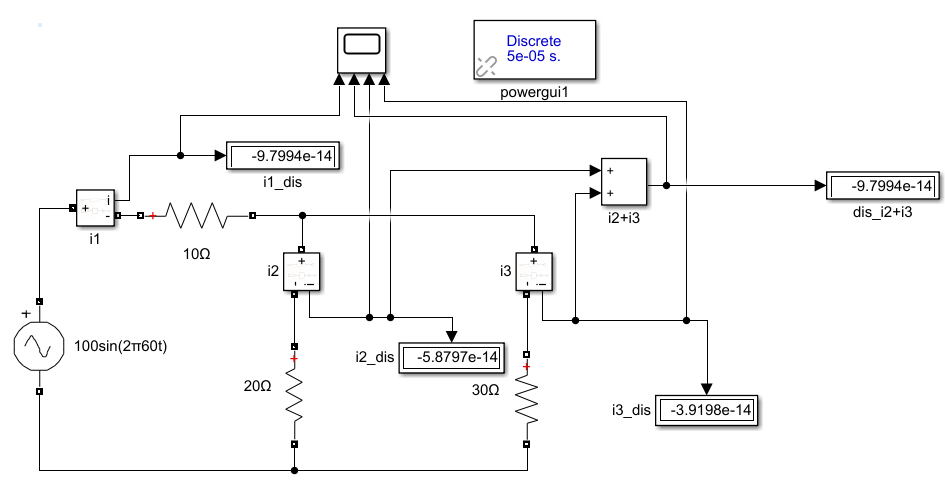
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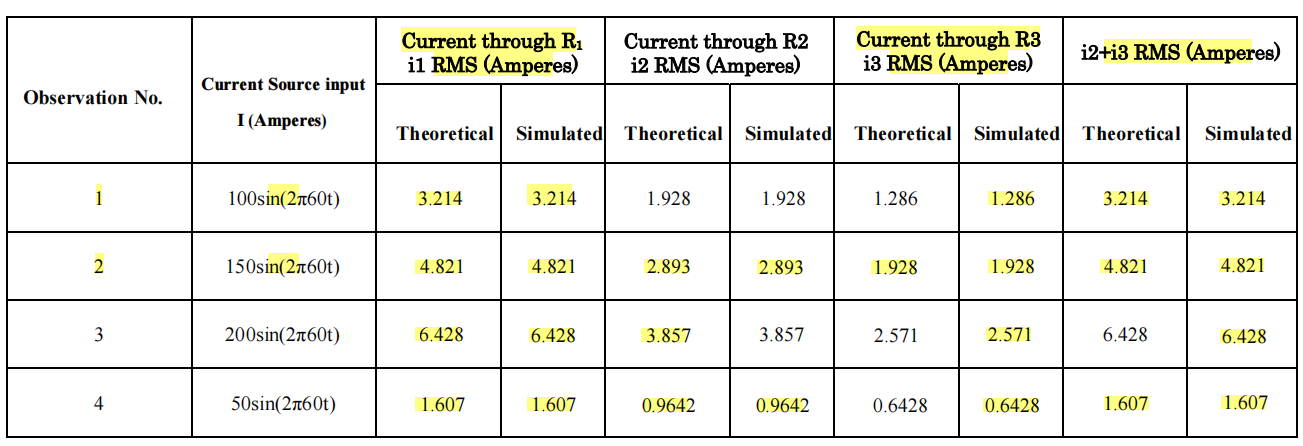
**Fig2h**: Circuit connections in Simulink for KVL using variable voltage source with ramp

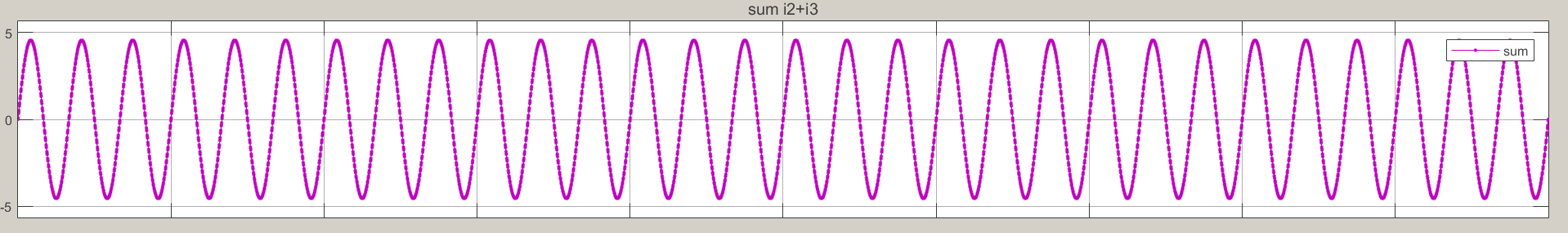
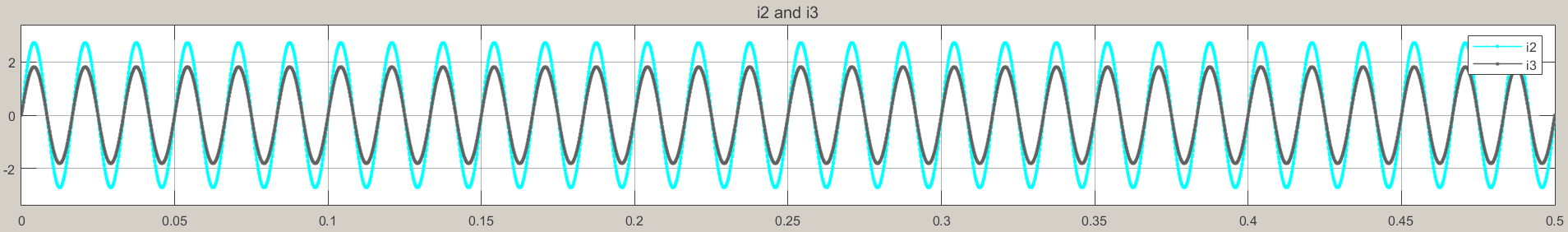
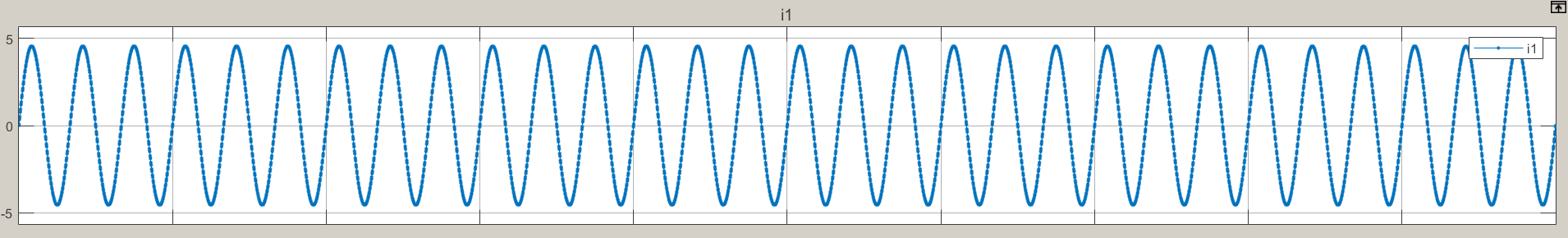
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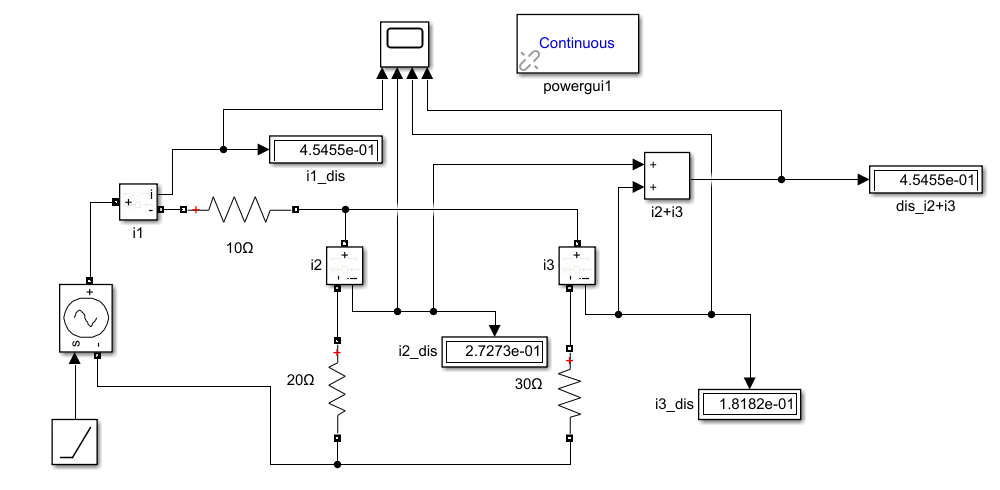
**Table2.6**: Observation table for KVL using variable voltage source with ramp

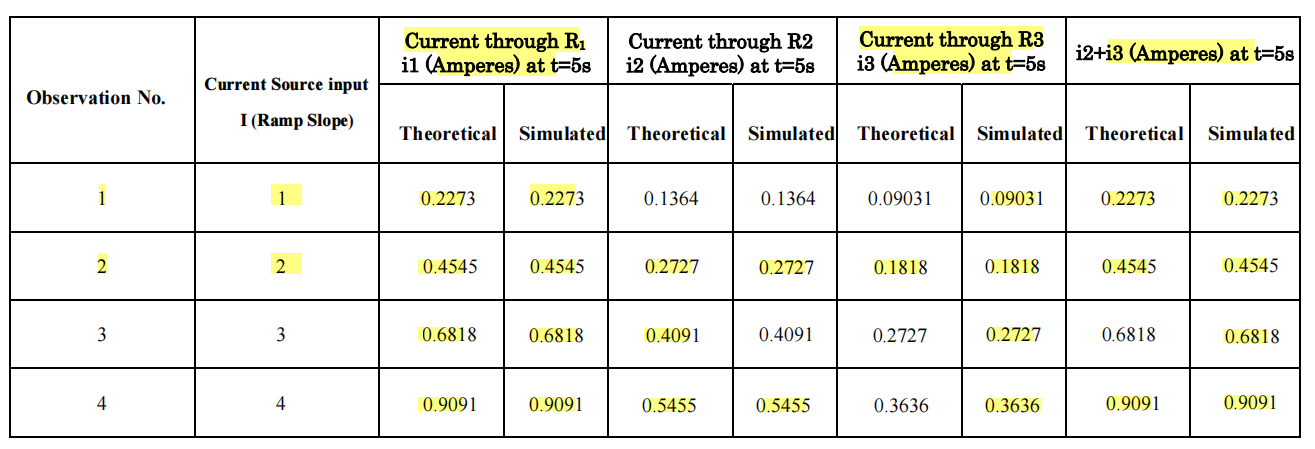
**Graph 2.2:** Graphical results of KVL using variable voltage source using ramp

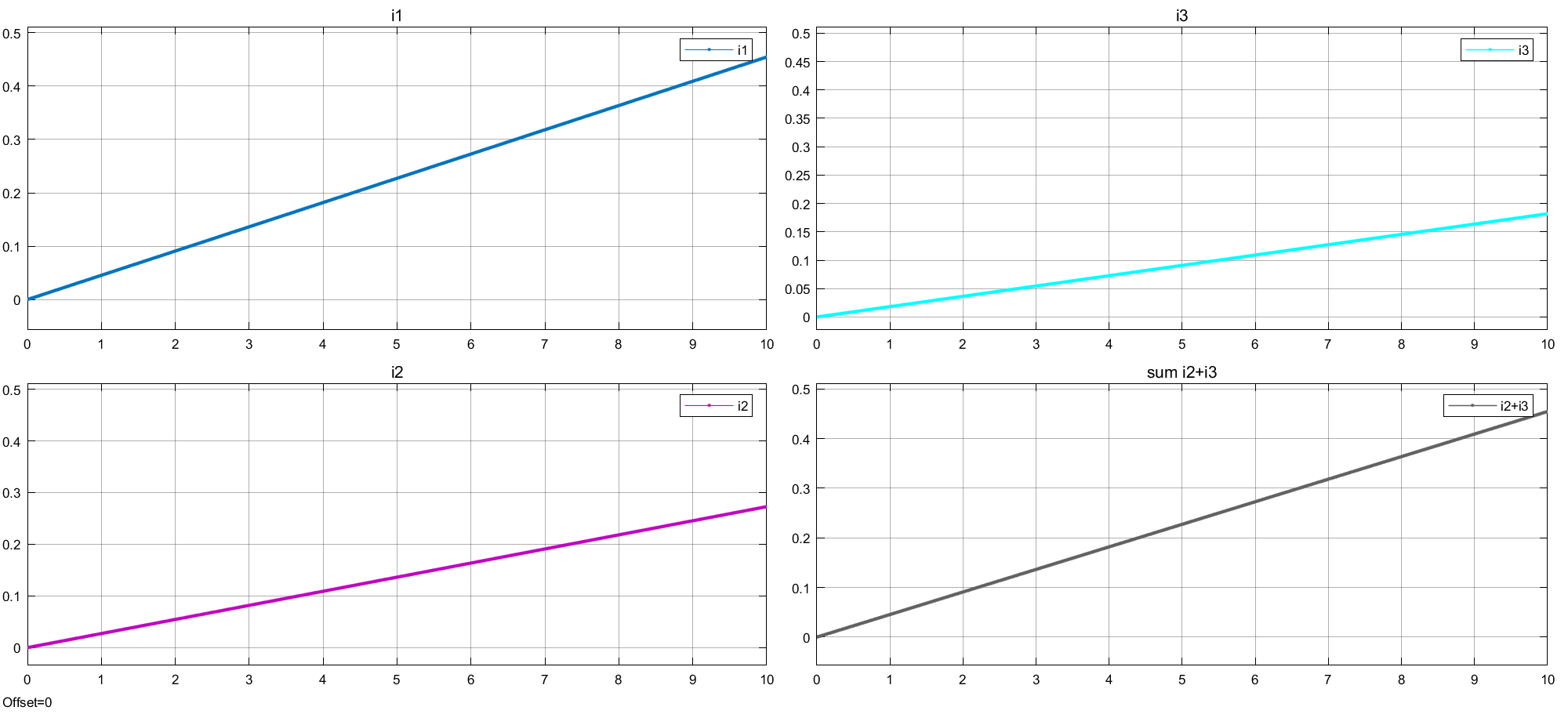
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**Fig2i**: Circuit connections in Simulink for KCL with sinusoidal voltage source**Table 2.7:** Observation table for KCL using sinusoidal current source

**Graph 2.3:** Graphical results of KCL using sinusoidal voltage source

  
 **Fig2j**: Circuit connections in Simulink for KCL using variable voltage source with ramp

**Table 2.8:** Observation table for KCL using variable current source with ramp



Sum i2+i3

i2

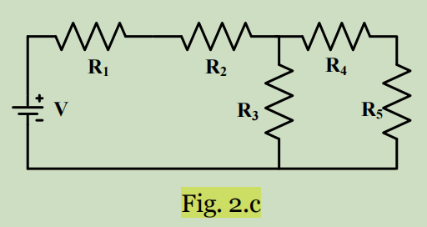
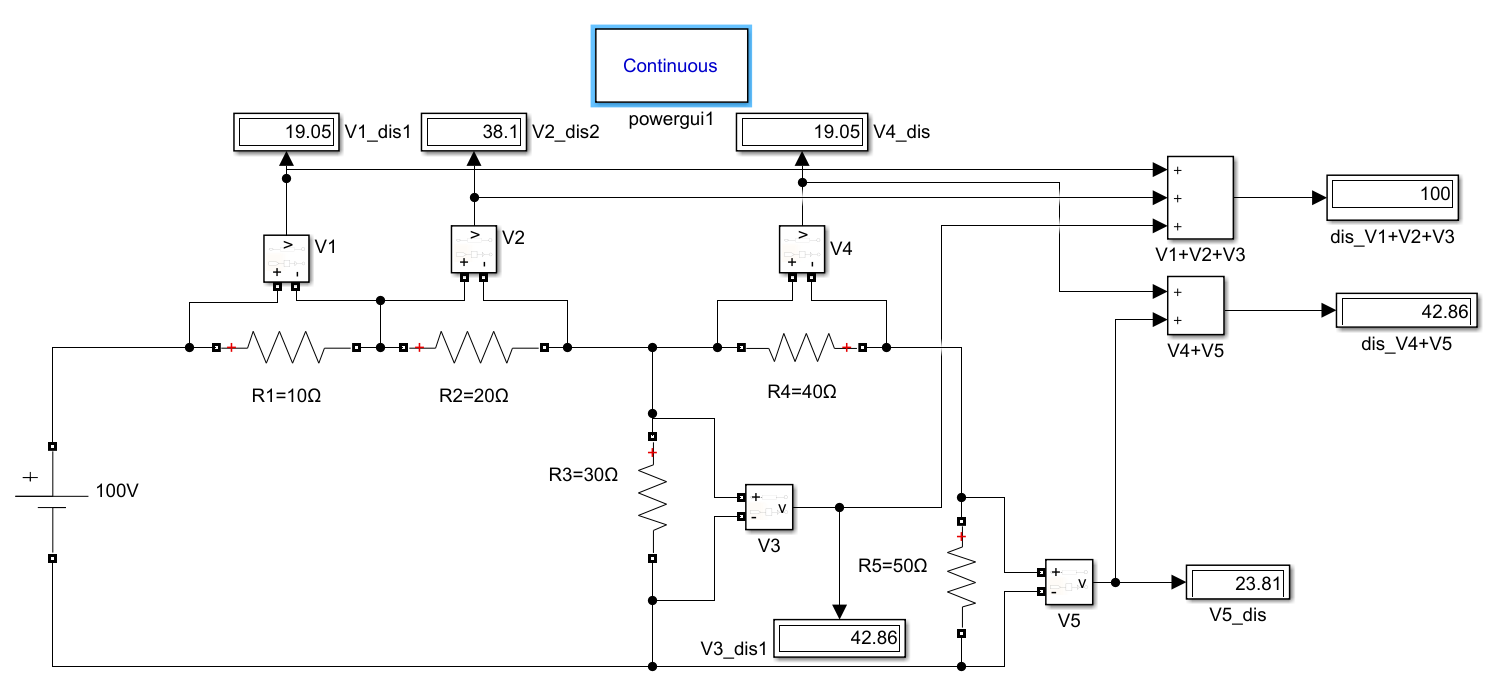
i1

i3

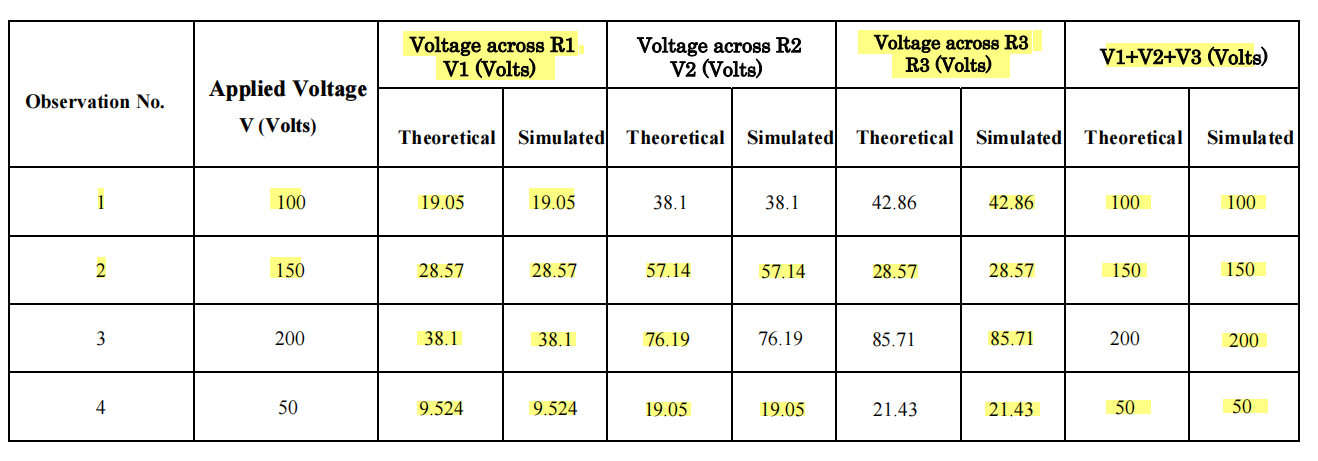
**Graph 2.4:** Graphical results of KCL using variable voltage source using ramp

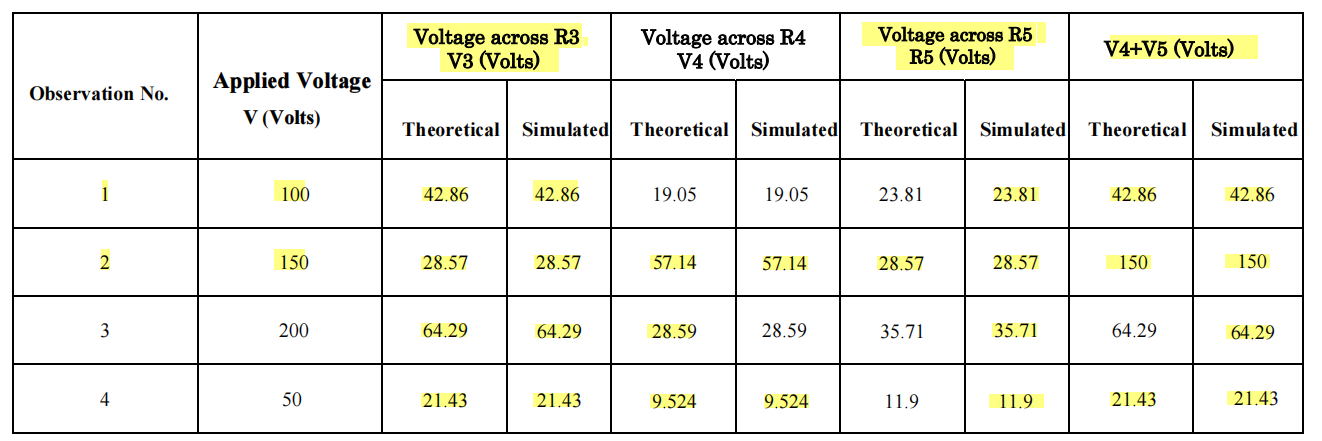
**Inferences**: From the observation table 2.5 & 2.6, it can be inferred that sum of V1+V2+V3 is always equal to V.

* From the observation table 2.7 & 2.8, it can be inferred that sum of i2+i3 is always equal to i1.
* All the theoretical readings match with the simulated readings.
* KCL and KVl is verified using variable voltage source such as voltage with constant slope and sinusoid voltage source.

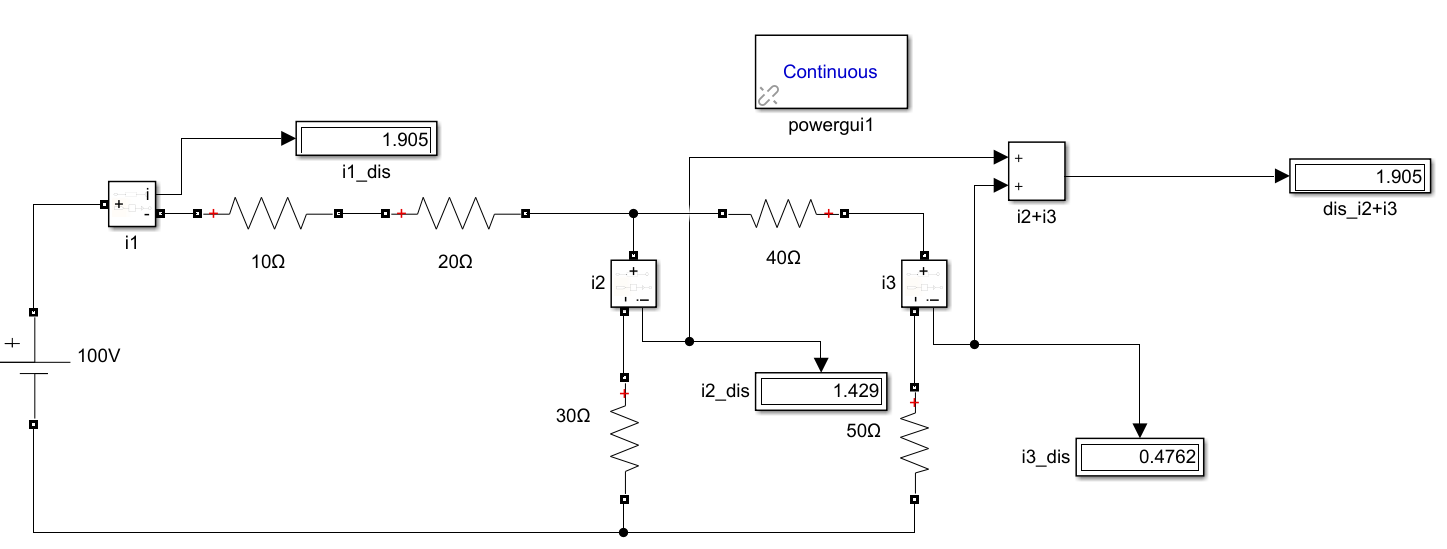
1. Using circuit shown in figure besides, do the experiment again. 

**Fig2k**: Circuit connections in Simulink for KVL

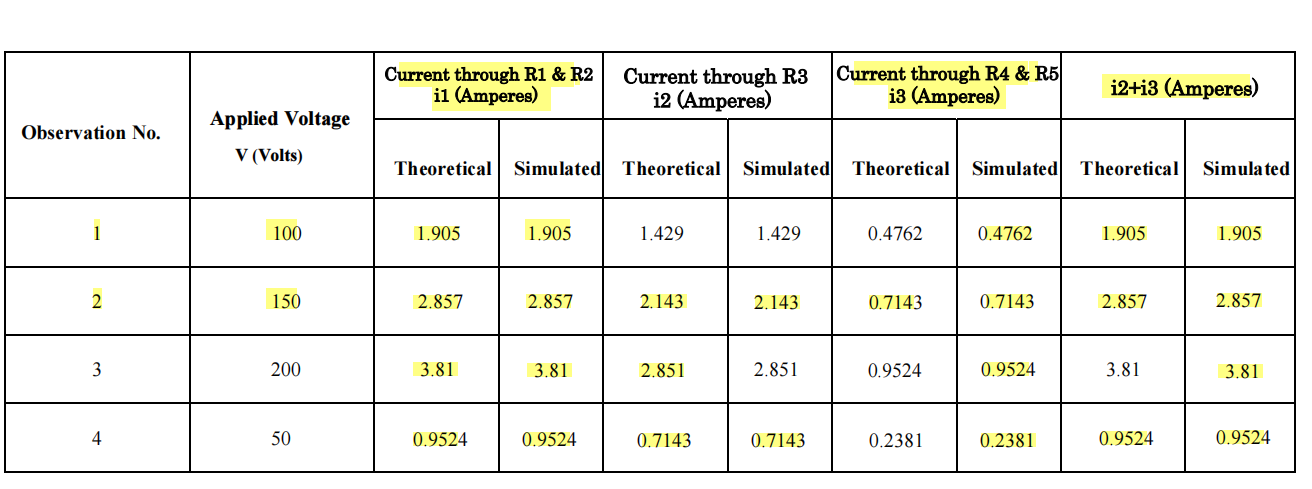
**Table 2.9:** Observation table for KVL for first loop



**Table 2.10:** Observation table for KVL for second loop



**Fig2l**: Circuit connections in Simulink for KCL



**Table 2.11:** Observation table for KCL using constant voltage source for ckt fig

**Inferences**:

* From the observation table 2.9, it can be inferred that sum of V1+V2+V3 is always equal to V.
* From the observation table 2.10, it can be inferred that sum of V4+V5 is always equal to V3.
* From the observation table 2.11, it can be inferred that sum of i2+i3 is always equal to i1.
* All the theoretical readings match with the simulated readings.
* KCL and KVL is verified for the given circuit.